CLAIMS

1. An apparatus for providing jitter measurement comprising:

a sampling circuit for sampling an input signal to obtain amplitude and phase information;

a computation circuit for computing Time Interval Error (TIE) information from the amplitude and phase information; and

a signal processor for determining a jitter spectrum from the TIE information.

2. The apparatus of Claim 1 further comprising a signal characteristics circuit for extracting characteristics of the input signal.

3. The apparatus of Claim 2 wherein the computation circuit uses the extracted characteristics in computing the TIE information.

4. The apparatus of Claim 2 wherein the signal characteristics circuit comprises:

a wideband clock recovery block for extracting a synchronous clock from the input signal;

a narrowband programmable Phase Lock Loop (PLL) for generating a sample clock from the synchronous clock;

a sampler for sampling the input signal using the sample clock to obtain signal samples;

an Analog to Digital (A/D) converter for converting the input samples to digital data; and

a Digital Signal Processor (DSP) for determining signal characteristics from the digital data.

5. The apparatus of Claim 4 wherein the narrowband programmable PLL comprises:

a reference divider receiving a recovered clock signal from the wideband clock recovery block;

a Voltage Controlled Oscillator (VCO);

a feedback divider receiving the output from the VCO;

a phase detector receiving the outputs from the reference and feedback dividers; and

a filter connecting the output from the phase detector to the input to the VCO.

6. The apparatus of Claim 5 wherein the VCO is a Hi-Q VCO.

7. The apparatus of Claim 5 wherein the VCO is a Voltage Controlled SAW (Surface Acoustic Wave) Oscillator (VCSO).

8. The apparatus of Claim 5 wherein the phase detector is a charge pump phase detector.

9. The apparatus of Claim 4 wherein the DSP determines high and low values from the digital data to compute high and low threshold values based on the high and low values and preset threshold fractions.

10. The apparatus of Claim 9 wherein the DSP: (i) groups the digital data based on whether the digital data is associated with rising or falling edges of the input signal, (ii) averages the digital data in both groups that falls within the high and low threshold values, and (iii) stores the result in appropriate look up tables corresponding to the rising or falling edge groups.

11. The apparatus of Claim 1 wherein the sampling circuit includes a Track and Hold (T/H) sampler that receives the input signal and the sample clock delayed by a fixed delay and provides amplitude samples to an A/D converter that generates quantized amplitude values corresponding to the amplitude samples.

12. The apparatus of Claim 11 wherein the sampling circuit further includes a first flip-flop and a second flip-flop that receive the input signal, the first flip-flop receiving the sample clock delayed by an adjustable delay and the second flip-flop receiving the sample clock delayed by the adjustable delay and a one unit delay, the output from the first flip-flop corresponding to a sampled digital value of the input signal sampled before the quantized amplitude value and the output from the second flip-flop corresponding to a sampled digital value of the input signal sampled after the quantized amplitude value, the digital sample values corresponding to the phase of the input signal.

13. The apparatus of Claim 12 wherein the flip-flops are thermally coupled with a heat sink to maintain their timing requirements over a wide temperature range.

14. The apparatus of Claim 12 wherein a delay control circuit adjusts the adjustable delay such that the digital values are sampled one half of a unit interval before and after the amplitude value is sampled.

15. The apparatus of Claim 12 wherein the T/H sampler and the A/D converter receive the sample clock delayed by the adjustable delay.

16. The apparatus of Claim 15 wherein the delay control circuit adjusts the adjustable delay such that the digital values are sampled one half of a unit interval before and after the amplitude value is sampled.

17. The apparatus of Claim 1 wherein the sampling circuit includes first and second T/H samplers that receive the input signal, the second T/H sampler receiving a sample clock delayed by one half of a unit interval from the sample clock provided to the first T/H sampler.

18. The apparatus of Claim 17 wherein: (i) the outputs from the T/H samplers are input to a comparator, (ii) the comparator outputs a digital value corresponding to the phase of the input signal sample, and (iii) an A/D converter receives the output from the first T/H sampler and generates a quantized amplitude value corresponding to the sampled input signal.

19. The apparatus of Claim 17 wherein the sampling circuit includes a first A/D converter that receives the output from the first T/H sampler and a second A/D converter that receives the output from the second T/H sampler, the outputs to the A/D converters corresponding to quantized amplitude values of distinct input signal samples.

20. The apparatus of Claim 19 wherein the quantized amplitude values are provided to the DSP which computes the phase corresponding to either quantized amplitude value.

21. The apparatus of Claim 1 wherein the signal processor performs further analysis including determining peak-to-peak jitter or a ratio of random to deterministic jitter.

22. The apparatus of Claim 1 wherein the computation circuit includes lookup tables providing a measured index based on the quantized amplitude value input to the lookup tables.

23. The apparatus of Claim 22 wherein the computation circuit further includes a differentiator finding the difference between the measured index associated with a current quantized amplitude value from a current ideal index.

24. The apparatus of Claim 23 wherein the computation circuit computes the current ideal index corresponding to a time domain fraction of the unit interval of a single cycle of the input signal, by adding a previous ideal index to the fractional part of the decimal number obtained by multiplying a ratio of the input signal frequency to the sampling clock frequency by the sample order of the input signal data registered in an internal counter.

25. The apparatus of Claim 24 wherein the computation circuit computes the current ideal index using a ratio of the input signal frequency to the sampling clock frequency such that the inverse of the ratio is a prime fraction.

26. A method for measuring jitter comprising:

sampling the input signal to obtain amplitude and phase information corresponding to the input signal;

computing TIE information from the amplitude and phase information corresponding to the input signal;

analyzing the TIE information to determine a jitter spectrum.

27. The method of Claim 26 further comprising extracting characteristics from the input signal for use in computing TIE information comprising:

extracting a synchronous clock from the input signal;

generating a sample clock from the synchronous clock;

sampling the input signal upon receiving sample clock signals;

converting the samples to digital data; and

determining signal characteristics from the digital data.